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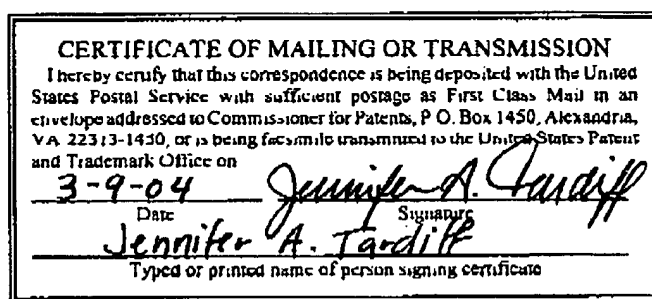
**FACSIMILE FILING OF PTO DOCUMENT****Examiner:** Andrew Q. Tran **Group:** 2824**Date:** March 9, 2004**Client Code:** 2037**Facsimile No.:** Corrected Filing Receipt Requests - 703-746-9195**From:** James M. Smith, Esq.**Subject: Paper:** Second Request for Corrected Filing Receipt**Docket No.:** 2037.1005-002**Applicant:** Peter B. Gillingham**Serial No.:** 09/654,367**Filing Date:** September 1, 2000**Number of pages including this cover sheet:** 6**Please confirm receipt of facsimile:** Yes X No    **Comments:**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Peter B. Gillingham  
Application No.: 09/654, 367 Group: 2824  
Filed: September 1, 2000 Examiner: Andrew Q. Tran  
Confirmation No.: 8231  
For: METHOD OF MULTI-LEVEL STORAGE IN DRAM AND  
APPARATUS THEREOF



SECOND REQUEST FOR CORRECTED FILING RECEIPT  
FOR UTILITY APPLICATION

Office of Initial Patent Examination  
Customer Service Center  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

We hereby request that the following items of information be corrected in the Filing Receipt for the subject application received in this office on February 26, 2004.

The errors and corrections appear below.

09/654,367

-2-

**Continuing Data as Claimed by Applicant Section**

This application is a REI of 08/595,020 01/31/1996 PAT R,E37,072

**SHOULD READ AS FOLLOWS:**

This application is a CON of REI 08/595,020 01/31/1996 PAT RE37,072, based on PAT 5,283,761.

Enclosed are a copy of the Filing Receipt with changes noted in red, and a copy of page 1 of the application as filed on September 1, 2000.

Pursuant to instructions in the February 29, 2000 O.G., we hereby request that the errors which are identified above be corrected in the captioned application to which this request for correction is directed. It is understood that the Patent Office will issue an automatically-generated, corrected Filing Receipt in this and, if applicable, any other affected applications.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By 

James M. Smith

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Date: 

**COPY**

## UNITED STATES PATENT AND TRADEMARK OFFICE

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APPL NO	FILING OR 371 (C) DATE	ART UNIT	FIL FEE RECD	ATTY DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
09/654,367	09/01/2000	2824	690	2037.1005-002	5	10	2

CONFIRMATION NO. 8231

CORRECTED FILING RECEIPT



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Date Mailed: 02/26/2004

Receipt is acknowledged of this reissue Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

## Applicant(s)

Peter B Gillingham, Kanata, ON, CANADA;

## Domestic Priority data as claimed by applicant

~~This application is a REI of 08/595,020 01/31/1996 PAT RE37,072~~

This application is a CON of REI 08/595,020 01/31/1996 PAT RE37,072, based on  
 Foreign Applications PAT 5,283,761.

If Required, Foreign Filing License Granted: 02/03/2001

Projected Publication Date: None, application is not eligible for pre-grant publication

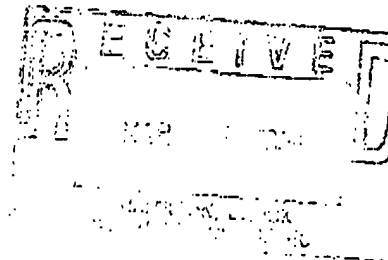
Non-Publication Request: No

Early Publication Request: No

## Title

Method of multi-level storage in DRAM and apparatus thereof

## Preliminary Class



365

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Title 37, Code of Federal Regulations, 5.11 & 5.15**

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**COPY****METHOD OF MULTI-LEVEL STORAGE IN DRAM**

This is a continuation of Reissue Application Ser. No. 08/595,020, filed January 31, 1996, which is based on original U.S. Pat. No. 5,283,761 issued February 1, 1994.

**FIELD OF THE INVENTION**

This invention relates to dynamic random access memory (DRAM) memories, and in particular to a method of storing a variable level signal in each cell of a DRAM for representing more than one bit in each cell.

**BACKGROUND TO THE INVENTION**

To store for example two bits in a DRAM cell, it must be able to store four different voltage levels. A problem with such cells, is that noise margins are reduced to one-third that of a one bit per cell DRAM, which is too low to withstand the occasional  $\alpha$ -particle hit.

A second problem with multi-bit storage cells relates to the method of sensing. No simple method of sensing has previously been designed, although attempts have been made to solve this problem, e.g. as described in the publication by M. Aoki et al, "A 16-Levels/Cell Dynamic Memory", ISSCC Dig. TECH. Papers 1985, pp. 246-247, and in T. Furuyama et al, "An Experimental Two-Bit/Cell Storage DRAM for Macrocell or Memory-On-Appliation", IEEE Journal of Solid State Circuits, Vol. 24, No. 2, pp 388-393, April 1989. The technique described by Aoki cannot use normal sense amplifiers. It requires a precision analog D to A converter to implement a staircase waveform and a charge amplifier to sense data. The technique described by Furuyama requires the generation of precision reference levels to distinguish between four levels. These levels are not self-compensated for offsets developed in the sensing operation, and this method suffers from poor signal margin. Hidaka et al describe a technique for simultaneously reading two cells at a time in the article "A divided/Shared Bitline Sensing Scheme for 64Mb DRAM Core" in the 1990 Symposium on VLSI Circuits 1990, IEEE, p. 15, 16 which while describing dividing a bitline, is not related to multiple bit storage in a single cell.

DRAMs have previously been built with cells holding up to sixteen bits of storage, e.g. in the aforementioned article by M. Aoki et al, for use in file memories. A 4 K test array is believed to have been the largest memory built using this design. Leakage characteristics of the DRAM cell were required to be very tightly controlled and even then, accurate sensing of the small voltage differences between levels becomes very difficult. Another problem with this scheme was the length of time required to access: a single read cycle required 16 clocks for the read followed by 16 clocks for the restore.

To implement a 2 bit DRAM, one can define the cell as storing one of four voltage levels  $V_{cell1}$ ,  $V_{cell2}$ ,  $V_{cell3}$  and  $V_{cell4}$ , and reference voltage midpoints between these four voltage, which can be defined as  $V_{ref1}$ ,  $V_{ref2}$  and  $V_{ref3}$ . These midpoints can be referred to, to differentiate between the four voltage levels. The relative voltage of these levels are shown in Table 1 below.

STORAGE VOLTAGES	REFERENCE VOLTAGES	ACTUAL VOLTAGE
$V_{cell1}$	$V_{ref3}$	$V_{DD}$
		$5/6 V_{DD}$
$V_{cell2}$		$2/3 V_{DD}$